REMARKS

Claims 1-4, 6-15 and 17-19 remain in this application. Claim 15 has been amended. Claim 20 has been cancelled. Claims 1, 9 and 15 are independent claims.

In the Office action dated September 7, 2005, it was noted that Applicant's previously filed remarks were moot in view of the new grounds of rejection. Accord to the new grounds of rejection, claims 1-4, 6-15 and 17-20 were rejected under 35 U.S.C. 103(a) as allegedly being unpatentable over Takinosawa in view of Douskey et al. (hereinafter "Douskey"). In response, Applicant has amended independent claim 15 to more particularly distinguish the claimed invention from the cited prior art. Amended claim 15 describes a method of testing operations of serializer/deserializers (SERDESs) of an integrated circuit. The method includes embedding a plurality of test interfaces within the integrated circuit such that each test interface is specific to one of said SERDES with respect to exchanging parallel data. Each test interface includes a test pattern generator connected to parallel data inputs of the SERDES to which the test interface is specific. Additionally, each test interface includes an error detector to receive parallel data from the SERDES to which the test interface is specific. Claim 20 has been cancelled. It is respectfully asserted that even if one were to modify the teachings of the primary reference to Takinosawa as proposed in the Office action, the resulting method would not render amended claim 15 obvious under Section 103(a).

Reconsideration of the claims in view of the amendment and in view of the remarks that follow is respectfully requested.

A. Overview of the Teachings of Takinosawa and Douskey

The invention of Douskey relates to a "system on a chip." This is described in the second paragraph of the patent (column 1, lines 17-33). A "system on a chip" may include a microprocessor, a memory, a bus interface and a memory controller. Advances in chip density permit all of these functions to be integrated onto the same integrated circuit device. Fig. 2 of Douskey illustrates a "system on a chip." Each core (60) may provide one of the functions of the "system on a chip." As described in column 6, lines 32-42, the different cores may be a processor core, an embedded memory, an input/output interface core, a memory interface, etc.

Regarding Takinosawa, the invention of the prior art reference relates particularly to testing the operation of a serial interface utilized in the implementation of a USB system (see Takinosawa at paragraph [0001]). As noted in paragraph [0002] of Takinosawa, the use of a USB for coupling a peripheral device to a host computer/controller has become well known. Applicant notes that it is common for a printer to be connected to a computer via a USB coupling.

The rejection of the claims is based upon the obviousness of incorporating the invention of Takinosawa into each core (60) of Douskey. Applicant respectfully asserts that it would not be obvious to incorporate a USB interface into each of a plurality of the cores of Douskey. Within the "system on a chip" of Douskey, the processor core may access data from the memory core via the memory interface core, but a person of ordinary skill in the art would not find it obvious to link the cores in the manner that an external printer is connected to a computer.

B. The Teachings of Takinosawa Regarding "a Plurality of SERDESs"

The Office action agrees that Takinosawa does not explicitly teach "a plurality of SERDESs," or "a plurality of functionally identical testers," or "each said tester is connected to a common test bus that is integrated with said SERDESs and said testers." Thus, Douskey is cited. On page 3 of the Office action, it is asserted that Douskey teaches an integrated circuit device (50) that includes a plurality of cores (60) (a plurality of SERDESs and a plurality of functionally identical testers) interconnected via one or more functional interfaces. Then, on page 4 of the Office action, there is a conclusion that Douskey "further teaches each said tester is connected to a common test bus that is integrated with said SERDESs and said testers." It is then concluded that the combination of Takinosawa and Douskey renders Applicant's claimed invention unpatentable because Douskey allegedly "teaches in an analogous art each of said testers being enabled to detect performance characteristics of individual said SERDESs independently of other said testers."

From the language in the Office action, it is clear that a *prima facie* case of obviousness exists only if Douskey teaches that the cores of Douskey include a plurality of SERDESs and a plurality of functionally identical testers. Applicant has carefully reviewed the Douskey patent and can find no support for concluding that the cores of Douskey include a

plurality of SERDESs. As previously noted, Douskey teaches a "system on a chip." The cores may include a processor core, an embedded memory, an input/output interface core, and a memory interface (Douskey: column 6, lines 32-35). The only references to SERDESs appear to be in claim 42 of the patent and in column 8, lines 1-9. Generally, a core interface unit (CIU) is close to its associated core. Thus, for cores that are located far from the master interface unit (MIU), it may be desirable to serialize the CIUs coupling to the bus (74). This is shown at serial line (78) in Fig. 3 of the Douskey. It may be desirable for relatively long runs of the bus (74) to be serialized so that the number of conductive traces routed over the long run is minimized. As shown in Fig. 3 of the patent, the SERDESs are not within the CIU (88). Equally importantly, the SERDESs of Douskey are not tested. That is, the "testers" of Douskey are not enabled to detect performance characteristics of individual said SERDESs, as set forth in Applicant's pending claim 1.

If it is asserted that Douskey indeed explicitly teaches SERDESs within the cores (60), Applicant requests citation of the explicit teaching within Douskey. On the other hand, if it is asserted that a plurality of the cores inherently include SERDESs, Applicant respectfully disagrees. A person of ordinary skill in the art would recognize that it is not inherent to require recurring serialization and deserialization when a processor core accesses information from a memory core via a memory interface core.

Applicant asserts that since neither Takinosawa nor Douskey teaches or suggests a plurality of SERDESs and a plurality of functionally identical testers connected to individually test each SERDES to detect performance characteristics of the individual SERDESs, a *prima facie* case of obviousness is not established by the combination of Takinosawa and Douskey.

C. Patentability of Independent Claim 1

Claim 1 describes an integrated circuit comprising (1) a plurality of SERDESs and (2) core processing logic integrated with each said SERDES and connected to each said SERDES to exchange signals therewith. In the primary reference to Takinosawa, there is a single "core," while Douskey was cited for teaching multiple cores. However, even if there were a separate SERDES for each core, as proposed in the Office action, the core processing logic would not be integrated with each SERDES and would not be connected to each SERDES to exchange signals therewith.

Claim 1 states that the integrated circuit also includes a plurality of functionally identical testers. The Office action correctly notes that Takinosawa does not teach a plurality of functionally identical testers. Therefore, Douskey is cited and it is asserted that the prior art reference includes a plurality of functionally identical testers. Applicant notes that the testers as taught by Douskey are shown in various drawings. The first of these drawings is Fig. 3. The uppermost tester (80) is a logic built-in self-test (LBIST) circuit which is used to pass pseudo random test patterns through logic gates to verify their correct operation. The second tester (82) is used for memory arrays. The second tester is an array built-in self-test (ABIST) circuit which may be used to apply test patterns through array elements to verify their operation. A third tester (84) is identified as a technical functional controller that provides technology-dependent functions, such as could be used to customize a device for different applications. Finally, a clock interface controller (86) is shown. In the description of Fig. 3 within column 7 of Douskey, these different options are found in different core interface units (CIUs). That is, the separate CIUs do not include each of the testers. Applicant asserts that Douskey does not teach or suggest a plurality of functionally identical testers.

D. Patentability of Independent Claim 9

Claim 9 describes an integrated circuit as including a plurality of functional test interfaces (FTIs) which are enabled to individually and concurrently test performances of the SERDESs. Each FTI is uniquely associated with one SERDES. As previously noted, it is agreed that Takinosawa does not teach a plurality of SERDESs. Fig. 3 of Douskey shows a pair of SERDESs (76), but does not teach an FTI associated with each SERDES. Moreover, the performances of the SERDESs are not tested. Nor is there a teaching that it would be beneficial to test the performances of the SERDESs of Fig. 3 in Douskey.

On page 10 of the Office action, it is asserted that Douskey teaches "said FTIs being enabled to individually and concurrently test performances of said SERDESs." As support for this conclusion, the Office action points out that each core interface unit of Douskey is assigned a unique address. Applicant asserts that this does not show that the core interface units may be concurrently activated to enable concurrent testing of the performance of components. As shown in Fig. 3 of Douskey, each of the four

core interface units, referenced as 80, 82, 84 and 86, can be individually addressed. However, concurrent testing is not inherent and any testing of a SERDES is not described. As provided in paragraph [0024] of Applicant's specification as originally filed, enabling concurrent running of the testing of the embedded SERDESs allows detection of the effects of crosstalk and power supply variations. This capability is not rendered obvious by the combination of the two prior art references.

Applicant respectfully submits that without the aid of reading Applicant's pending application, the possibility of modifying either Takinosawa or Douskey in view of the other reference would not be apparent to a person of ordinary skill in the art. In fact, Applicant asserts that even with the aid of hindsight, it would not be obvious to modify Takinosawa in view of Douskey to provide the integrated circuit described in claims 9-14.

E. Patentability of Independent Claim 15

As previously described, claim 15 has been amended to more clearly distinguish the claimed invention from the cited prior art. The step of embedding the plurality of test interfaces includes forming each test interface to include a test pattern generator connected to parallel data inputs of the SERDES to which the test interface is specific. The step of embedding the test interfaces also includes forming each test interface to include an error detector to receive parallel data from the SERDES to which the test interface is specific.

Many of the remarks made above apply to the determination of patentability of independent claim 15. Firstly, it would not be obvious to modify Douskey to include the USB capability of Takinosawa for each core within the system on a chip. Additionally, it is neither taught in nor inherent to the "system on a chip" to include a plurality of SERDESs. Additionally, the arrangement of the various components for testing is not obvious in view of the combination of the two prior art references.

Applicant respectfully requests reconsideration of the claims in view of the amendments and remarks made herein. A notice of allowance is earnestly solicited. In the case that any issues regarding this application can

be resolved expeditiously via a telephone conversation, Applicant invites the Examiner to call Terry McHugh at (650) 969-8458.

Respectfully submitted,

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